Mitigating TSV-induced Substrate Noise in 3-D ICs using GND Plugs

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Abstract

Through-silicon vias (TSVs) in 3-D ICs are a major source of substrate noise, causing performance degradation of neighboring active devices. To reduce this noise, we propose using a tungsten-filled *ground plug*, a TSV-like structure that connects to ground (GND) and that partially or completely extends through the substrate. We evaluate the impact of plug size and placement on noise isolation. We compare the GND plug technique with two other noise mitigation techniques: using a thicker dielectric liner and using a backside ground plane. Our study demonstrates that the GND plug is a superior technology, effective in mitigating TSV-induced substrate noise by an order of magnitude when compared to the other two techniques. The GND plug offers a more practical noise isolation approach than using a backside ground plane. When compared with increased dielectric thickness, the GND plug offers a 33% reduction in foot print and permits a significantly reduced keep out zone.

Keywords

3-D integrated circuit (IC), 3-D integration, through-silicon via (TSV), substrate noise.

1. Introduction

Three dimensional (3-D) integration technology offers unique opportunities to create a system-in-package (SiP) with improved performance and heterogeneous integration. Dies from disparate technologies (analog, digital, mixed signals, sensors, and antenna) and from different technology nodes can be stacked to form a 3-D SiP with higher bandwidth, low latency, low device power, and small form factor [4,7,13]. Wire bonding and through-silicon vias (TSVs) are two stacking techniques to create 3-D ICs. TSVs offer reduced delay and power, and increased connectivity when compared to the connections possible with wire bonding [10]. At the same time, TSVs are a major source of substrate noise that threatens the performance of neighboring devices. In addition, TSV noise increases leakage current, which increases static power consumption and can erroneously turn transistors from the "off" state to the "on" state [15]. A "keep out" zone, specified through layout rules, is thus required to shield devices from neighboring TSVs.

We propose in this paper a practical and effective device, a ground (GND) plug, to reduce TSV-induced substrate noise. A GND plug is a TSV-like structure that is connected to circuit ground and may extend partially or completely through the substrate. Multiple GND plugs, fabricated around a TSV, provide noise isolation between TSVs and neighboring devices. We propose Tungsten (W) as fill material for two reasons. First, a smaller CTE (Coefficient of Thermal Expansion) mismatch of W and Silicon (Si), compared to Copper (Cu) and Si, will result in less thermal stress in devices. Second, W does not require any diffusion barrier like Cu and will provide a direct connection between substrate and circuit ground resulting in better device shielding. A GND plug is different from a GND substrate tie that provides typical substrate or well ties without much depth into the substrate.

We examine in this paper the physical design and placement of GND plugs for effective noise isolation. We compare the GND plug technique with two other noise mitigation techniques: thicker dielectric liner and backside ground plane. Thicker dielectric liner provides shielding which decreases coupling between TSV and substrate. A backside plane, electrically connected to circuit GND, ensures sufficient substrate grounding. Our results show that GND plugs provide excellent TSV substrate isolation at smaller area penalty. Our contributions are:

- We propose an effective technique to mitigate TSV-induced substrate noise.
- We study the size and placement considerations of GND plugs to maximize noise isolation and to minimize area penalty.
- We compare the performance and area penalty of GND plugs with thicker dielectric liner and backside ground plane.
- Our analysis framework is realistic and uses finite-element based three-dimensional extraction tool to extract lumped parasitics for our experimental design setups.
- More importantly, we show that the GND plug provides a superior advantage in reducing substrate noise while utilizing small area and minimizing the keep out zone.

The rest of the paper is organized as follows. We present an overview of TSV-induced noise and related work in Section 2. We describe our evaluation framework used to perform lumped parasitic analysis in Section 3. We perform a comparison of three different noise mitigation techniques, thicker dielectric liner, backside ground, and GND plugs in Section 4, and we conclude our study in Section 5.

2. Overview of TSV-induced noise and related work

TSV is a metallic (usually Cu) wire extending throughout the substrate and isolated by dielectric and barrier materials. Figure 1 shows a cross-section view of an Si substrate with a TSV and a MOSFET transistor. Signal transitions through a TSV create noise that can pass through the substrate and

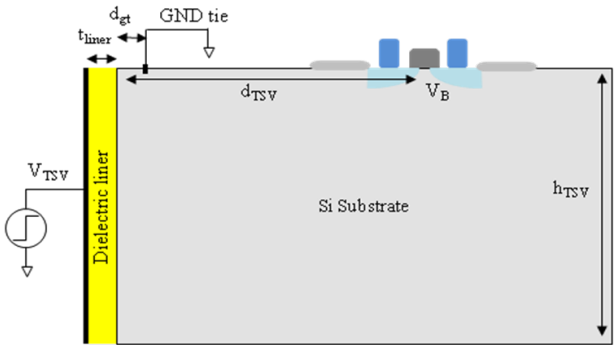


Figure 1: Cross-section view illustrating TSV-to-device coupling.

impact the performance of neighboring active devices and TSVs. Physical design considerations (see Figure 1) that can be exploited to mitigate TSV-induced substrate noise include dielectric liner thickness (t_{liner}), TSV-to-device distance (d_{TSV}), and GND ties (conventional substrate ties, often referred to as substrate contacts). Figure 2 shows variations in the device body voltage, V_B, at different distances from a TSV for a set of design parameters. These transitions are short-lived and occur only with a change in the signal passing through a TSV. For a 1µm thick liner, the peak value of these transitions is significant (40% of VDD), despite including a GND tie 0.5µm from the TSV.

Substrate noise is a well-studied problem in traditional 2-D IC design [3]. While it has not been a serious concern in digital circuit design, analog circuit design has always been a subject of higher scrutiny for noise isolation. Several noise isolation techniques, including split power planes, deep-nwell process, and guard ring structure, have been employed in mixed-signal designs. For a 3-D IC design, this problem is not yet well addressed. The extent of TSV-induced substrate noise problem is directly related to the density of TSVs. Conventional noise mitigation techniques, such as isolated floorplanning of noise sensitive circuits with guard bands, are not feasible in 3-D design with the high density of TSVs as predicted by the ITRS roadmap [2].

While analog circuits are adequately guard banded for noise isolation, digital circuits in close TSV proximity are subject to TSV coupling noise due to full voltage swing

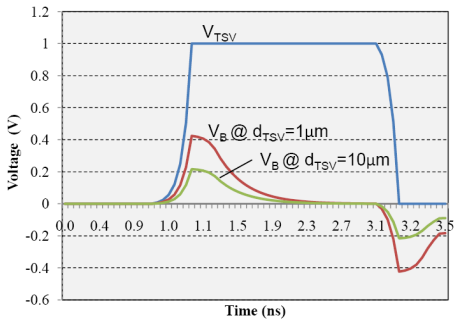


Figure 2: Body voltage during TSV signal transition at different TSV distances, d_{TSV} , for V_{TSV} =1V square wave, h_{TSV} =20µm, t_{liner}=1µm, d_{gt}=0.5µm, signal transition time=50ps [11].

levels in signal TSVs. To explore the impact of body voltage variations on device performance, we modeled a fan-out 4 inverter, in 32nm technology node. We vary the peak body voltage, keeping the waveform same as shown in Figure 2. The resulting variations in delay and dynamic power are shown in Figure 3. It is evident from Figure 2 and Figure 3 that TSV-induced noise plays a significant role in determining device performance.

A number of techniques have been identified for noise mitigation: thicker dielectric liner, backside ground plane [11], guard ring structure [5], and co-axial TSVs [9]. Increasing the thickness of the dielectric liner surrounding a TSV is the simplest approach. Increased liner thickness has already been shown to be insufficient in mitigating substrate noise [11]. Providing a backside ground by placing a die on a grounded metal sheet is a common strategy to mitigate substrate noise in 2-D ICs. This strategy may not be practical for 3-D ICs because of two reasons: 1) a metallic sheet between dies will introduce unnecessary inductive coupling, 2) design complexity will increase because TSVs passing through metallic sheets must be isolated. Surrounding TSVs with guard rings is not effective because typical guard-ring depth is comparable to GND tie depth, which is too small to provide any significant isolation [5]. Lastly, using a co-axial TSV is promising to mitigate noise but the manufacturability of co-axial TSVs is still in question.

We propose in this paper an alternative and more practical technique to reduce TSV-induced substrate noise by using tungsten (W)-filled GND plugs in the vicinity of TSVs. W-filled TSVs have been demonstrated for the fabrication of 3-D LSI chips [12]. Unlike TSVs, the proposed W-filled GND plugs may not extend through the complete depth of the substrate. Tungsten is not the preferred material choice for TSVs due to higher resistivity. However, W-filled plugs have the advantages of direct substrate connectivity without any barrier layer and higher RC damping for less noise transfer from the GND power supply. To quantify the effectiveness of the proposed W-filled GND plugs technique and to investigate some of the critical physical design parameters, such as their placement and height, we first develop a lumped parasitic analysis framework.

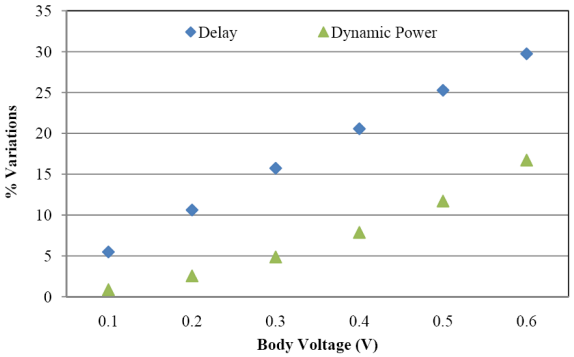


Figure 3: Variations in performance and power of a fan-out-of-four CMOS inverter in 32nm technology node due to body voltage noise.

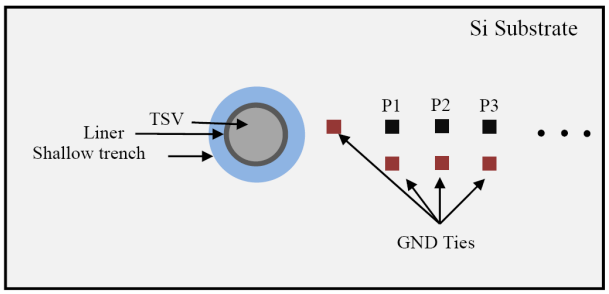


Figure 4: Top view of TSV-induced noise analysis framework. The voltage at the observation points, e.g. P1, P2, and P3, represent body voltages of neighboring transistors while the GND ties are their neighboring conventional substrate ties.

3. Evaluation framework for TSV-induced noise

Our evaluation framework is a three-dimensional structure comprising a Cu TSV in an Si substrate, ground ties, and voltage observation points. The top view of this setup is shown in Figure 4. Each component is defined below.

- **Substrate:** We assume a high-R substrate with a resistivity of 10Ω-cm and relative permittivity of 11.8. This type of substrate is used to fabricate low cost, low performance devices like memory [6].
- **TSV**: We assume a cylindrical Cu TSV. Its height is the same as the substrate height and the diameter is fixed to be 2µm (unless specified).
- **Dielectric Liner**: We use an SiO_2-based dielectric liner, with a resistivity of 10^{16}Ω-cm and relative permittivity 3.9, surrounding the TSV. The default thickness of dielectric liner is assumed to be 0.1µm which is consistent with recent design studies [8].
- **Shallow Trench:** Thermal stress is one of the most important factors shaping TSV technology. We assume an SiO_2 shallow trench. Its thickness and depth (into the top surface of substrate) are assumed to be 0.9µm and 0.3µm respectively. These values are consistent with those in the ITRS roadmap [2].
- **Observation Points:** We assume 9 equally spaced observation points (P1, P2, ...) located 4µm to 20µm away from the center of the TSV. These points are modeled as small metallic cubes to enable extracting parasitics between TSV and devices at various distances from the TSV.
- **GND Ties:** Placing GND ties throughout the circuit layout is the conventional approach to control transistor body voltages, and hence, is considered in our setup. We assume a GND tie at a distance of 0.3µm from the shallow trench edge. Also, we assume that there is at least one GND tie within a 1µm distance of each observation point. Note this GND tie is not the proposed W-filled GND plug.

Table 1: Critical parameters for our TSV-induced noise analysis framework.

Parameter	Value
Substrate height	20µm
Substrate length	50µm
Substrate width	50µm
TSV height	20µm
TSV diameter	2µm
Liner thickness	0.1µm
Shallow trench height	0.3µm
Shallow trench width	0.9µm
Resistivity of high-R substrate	10Ω-cm

Table 1 shows the default values of parameters in our TSV-induced noise analysis framework. These values should be assumed when any of the parameters is not being varied for sensitivity investigation. To extract an equivalent SPICE circuit for our framework, we use a finite-element based 3D extraction tool (Q3D Extractor) from Ansoft. Figure 5 shows a portion of the extracted circuit comprising a TSV, an observation point, a GND tie, and Si substrate. A step input, with a rise time of 100ps and peak voltage of 1V, is applied at one of the TSV terminals whereas the other terminal is assumed to be floating. We perform transient analysis and report peak noise at the observation points.

RLC values of the extracted circuit depend upon the extraction frequency. Q3D Extractor divides the frequency spectrum into DC, AC, and transition regions. In contrast to the AC region, the DC region does not account for any skin depth and relative frequency dependent parameters. The transition region, which spans about a decade of frequency, does not produce a valid solution because neither AC nor DC models are truly valid [1]. Before we perform any analysis, we extract the SPICE netlist for various values of operating frequencies (between 1KHz and 10GHz) using the default design parameters from Table 1. Due to relatively large dimensions of TSVs, in the order of µms, the DC region expands to well above 1GHz frequency and the RLC parameters are mostly unchanged in the DC region. We choose the operating frequency to be 1GHz for our analysis.

4. TSV-induced substrate noise analysis

We present in this section an analysis of different noise mitigation techniques. We investigate the impact of using

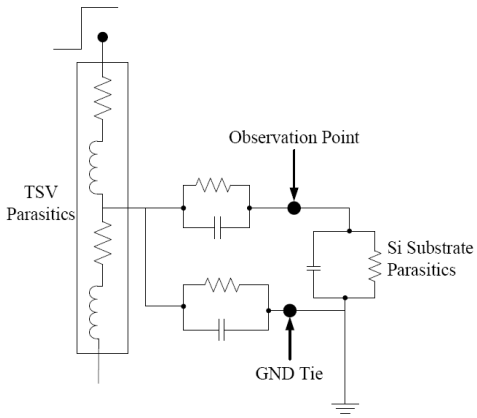


Figure 5: An example extracted circuit comprising TSV parasitics, a single observation point, a GND tie, and Si substrate parasitics for coupling among the three elements.

thicker dielectric liner and using a backside ground plane in Section 4.1 and Section 4.2 respectively. We present a detailed study of the proposed GND plug technology in Section 4.3. We compare the performance and area penalty of these three techniques in Section 4.4.

4.1. Using thicker dielectric liner

Increasing liner thickness is the simplest approach to mitigate TSV-induced substrate noise. We vary liner thickness from 0.1µm to 3µm in the default setup shown in Figure 4 and extract an RLC circuit for each setup using Q3D Extractor. SPICE is used to observe peak transient noise at various observation points in the substrate. Figure 6 plots peak transient noise for several liner thickness values at observation distances 6, 10, and 20µm from the TSV. We conclude the following:

- Peak transient noise ranges from 0.18V to 0.7V, regardless of distance from TSV, for all examined values of liner thickness. This indicates that standard GND substrate ties are inadequate for creating a reference GND substrate in the presence of TSV-to-substrate coupling. Hence, using GND substrate ties alone is not effective in mitigating TSV-induced noise.
- Peak substrate noise decreases with increasing liner thickness. This trend is not uniform and can be divided into three segments. The impact of increasing liner thickness is the maximum for liner thickness between 0.1µm and 1µm, reduces for liner thickness between 1µm and 2µm, and saturates after 2µm.
- Peak substrate noise is ~18% of VDD for liner thickness of 3µm, a huge area penalty for TSVs. This 6x area penalty, for 2µm diameter TSV, will create large interconnect blockages and will reduce the area used for active devices.

4.2. Using a backside ground plane

During assembly and packaging stages, a 2-D die is placed on a grounded metal layer. As mentioned in Section 2, the same idea can be extended to 3-D ICs where the substrate has a backside grounded metal, in preferable plate or grid format, creating a strong GND reference for substrate. To model this technique, we add a Cu sheet in the default setup shown in Figure 4. Sheet cross-section is the same as substrate cross-section and sheet thickness is

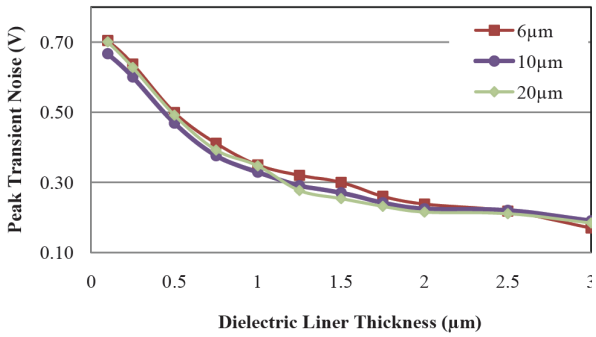


Figure 6: Impact of thicker dielectric liner: peak transient noise at different observation distances (6, 10, and 20 µm) from the TSV for increasing liner thickness.

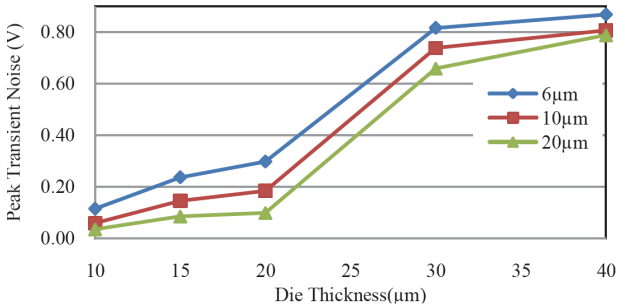


Figure 7: Impact of backside ground plane: peak transient noise at different observation distances (6, 10, and 20µm) for different die thickness (distance from device to backside ground) values.

assumed to be 2µm. One side of the sheet connects to the substrate and the other side connects to GND. Substrate thickness, the distance between devices layer and the backside ground, is the only variable of concern for substrate noise analysis. We vary the substrate thickness from 10µm to 40µm and extract the RLC circuit for each setup. We use SPICE to observe peak transient noise at the observation points. The results of this study are shown in Figure 7. We make the following observations:

- Unlike the thicker dielectric liner approach, substrate noise decreases as a function of TSV distance. Using the backside ground plane is more effective in localizing noise.
- Our results show that the capability of backside ground to mitigate substrate noise is a function of substrate thickness. The impact is minimal for larger values of thickness. Backside ground is therefore effective in technology generations where substrate heights can be aggressively reduced by substrate thinning.

4.3. Using Tungsten GND plugs

The analyses presented above show that both noise mitigation techniques have their performance and/or technology limitations. As an alternative technique, we propose using W-filled GND plugs and investigate the effectiveness of this technique. Figure 8 shows the design setup with added GND plugs. We first investigate the impact of placing different numbers of GND plugs. We evaluate the use of four GND plugs fabricated at 3µm from the center of TSV. Noise isolation is improved by 2.46x when compared

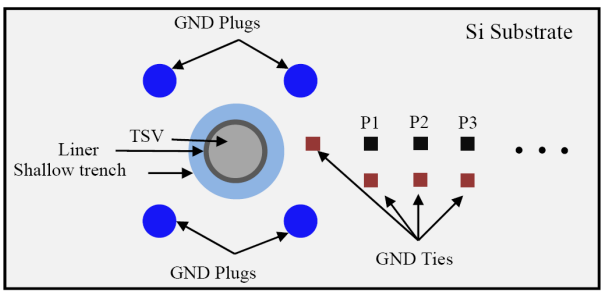


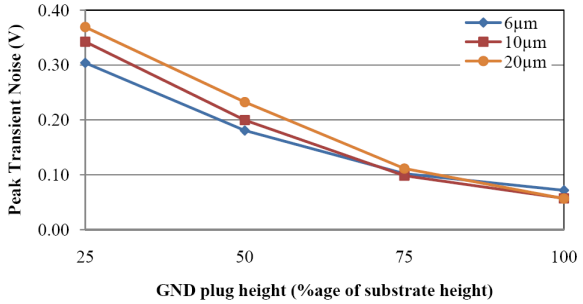
Figure 8:. Top view of TSV-induced noise analysis framework with GND plugs.

to using only two GND plugs. For the rest of the analysis, we therefore utilize four plugs. Next, we explore the impact of two critical parameters: plug diameter and plug depth. RLC circuits for each setting are extracted using Q3D Extractor and then simulated in SPICE for peak transient voltage at the observation points.

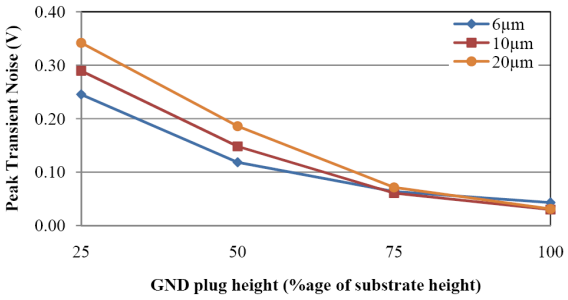
Figure 9 shows the peak transient noise for three different GND plug diameters with varying plug height. We make the following observations:

- GND plug is effective in reducing the peak noise. A deeper GND plug is more effective than a shallower one in reducing peak noise.
- The benefit of increasing plug diameter occurs at the expense of increased area with little benefit in noise reduction. For a 3x increase in plug diameter from 0.5µm to 1.5µm, noise reduction is only 10%.

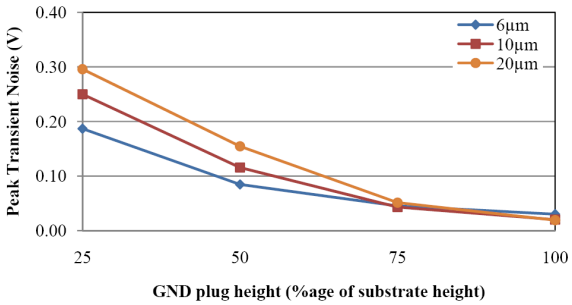
GND plug diameter and depth are related due to aspect ratio limitations of deep trench formation and filling in Si substrate. The results in Figure 9 suggest the need for small diameter yet deep GND plugs. Kikuchi et al. demonstrate W-filled TSV formation using deep-Si-trench etching and Tungsten chemical vapor deposition (CVD) where TSV diameter is maintained till 70% of substrate height for an aspect ratio of approximately 18:1 [12]. Interestingly, the proposed GND plug scheme does not require sidewall isolation nor high uniformity of plug diameter as a function of depth. A higher aspect ratio cone-shaped plug is thus possible, and warrants further investigation.



(a) Plug diameter = 0.5µm



(b) Plug diameter = 1µm



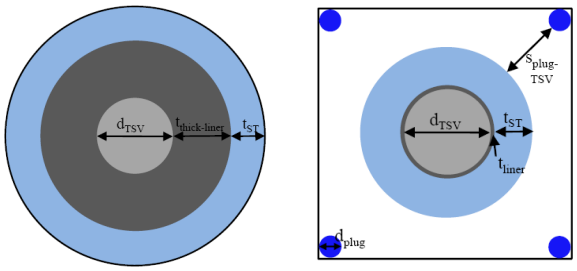
(c) Plug diameter = 1.5µm

Figure 9: Impact of GND plug height on peak transient noise at different observation distances (6, 10, and 20µm).

4.4. Comparison of three noise mitigation techniques

In addition to peak noise, area penalty and routing blockages are important comparison metrics of the three discussed noise mitigation techniques. We utilize the default design parameters described in Table 1 and explore the relative merits of the three techniques. In the thicker dielectric liner approach, we assume the liner thickness to be 1.5µm. In the GND plug approach, we assume a 0.5µm diameter plug with the same depth as the substrate thickness. The top view TSV with thicker liner and TSV with GND plug is shown in Figure 10 to illustrate area penalty analysis.

Table 2 reports peak transient noise and substrate area blockages for different noise mitigation techniques along with the baseline TSV case where no noise isolation technique is applied. The peak noise is reported at 6µm, 12µm, and 18µm away from TSV center. The proposed GND plug technique with a 40:1 aspect ratio is superior in mitigating the TSV-induced substrate noise by an order of magnitude when compared to using thicker liner and backside ground approaches. The area penalty for the GND plug is smaller than the added area due to using a thicker liner. Fabrication of W-filled TSV with an aspect ratio of 50:1 and diameter of 1µm has been proposed [14], which suggests that the GND plug with a diameter of 0.5µm and an aspect ratio of 40:1 is achievable. We present the results for a smaller aspect ratio of 20:1 in Table 2. These results show that even the smaller aspect ratio yields 40% reduction in TSV-induced noise when compared to the other two approaches. If the desired substrate noise limit is 10% of VDD, then the GND plug with a height of 20µm is the only solution that meets the requirement. The resulting keep out



(a) Thicker Liner (b) GND plug

Figure 10:.Comparison of substrate area dedicated for thicker liner and GND plugs (d_{TSV} =2µm, $t_{thick-liner}$=1.5µm, t_{ST} =0.9µm, t_{liner}=0.1µm, $s_{plug-TSV}$ =1µm, and d_{plug}=0.5µm). The area penalty for the thicker liner is 36.3µm^2 and for the GND plug is 24.5µm^2

Table 2: Comparison of peak transient noise and relative area blockage for the three TSV-induced noise mitigation techniques.

Technology	Peak transient noise (V)			Substrate area blockage (Relative)
	6μm	12μm	18μm	
Baseline TSV (TSV height=20μm, liner thickness=0.1μm)	0.705 V	0.658 V	0.663 V	1
Thicker liner (1.5μm)	0.300 V	0.265 V	0.251 V	3.06
Backside ground plane for baseline TSV	0.298 V	0.098 V	0.155 V	1
GND plug (diameter=0.5μm, height=20μm) with baseline TSV	0.072 V	0.055 V	0.053 V	2.0
GND plug (diameter=0.5μm, height=10μm) with baseline TSV	0.181 V	0.206 V	0.216 V	2.0

zone considering TSV-induced noise is thus a square area of side 5μm. When using a thicker liner, a similar noise margin can only be attained using a liner thickness greater than 3μm, resulting in a keep out zone diameter in excess of 10μm. TSV-induced stress also contributes to the required keep out zone but it is not considered in our analysis.

5. Conclusion

We proposed a novel noise mitigation technique, the GND plug, and compared its effectiveness against two other noise mitigation techniques: thicker dielectric liner and backside ground plane. We assumed practical design parameters and utilized a three-dimensional finite-element based solver to extract the SPICE netlist of our experimental setup. Analysis of a 1.5μm -thick dielectric liner shows peak substrate noise of 30% of VDD, thus necessitating further increase in thickness or a significant increase in the keep out zone. Furthermore, the resulting area penalty, 3x the size of a 2μm diameter TSV, creates routing blockages and reduces the area available for active devices. While a backside ground plane or mesh is effective with thinned dies, placing such a metal sheet or mesh between dies in 3-D ICs may not be practical. We showed that a GND plug with an aspect ratio of 40:1 is effective in reducing noise by an order of magnitude with a smaller area penalty than a thicker liner. A GND plug with a smaller aspect ratio (20:1) provides 40% reduction in substrate noise when compared to the other two techniques. The proposed GND plug technique thus offers a practical and promising solution to the difficult problem of providing device shielding against TSV-induced substrate noise.

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